UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/782,612	02/19/2004	Joel F. Adam	6259P006	5142

8791 7590 02/04/2009

BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP
1279 OAKMEAD PARKWAY
SUNNYVALE, CA 94085-4040

EXAMINER	
FRANKLIN, RICHARD B	
ART UNIT	**PAPER NUMBER**
2181	

MAIL DATE	DELIVERY MODE
02/04/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/782,612	ADAM ET AL.	
	Examiner	Art Unit	
	RICHARD FRANKLIN	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 15-17* is/are rejected.

7)☒ Claim(s) *11-14 and 18-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 – 20 are pending.

Oath/Declaration

2. The oath/declaration has been reviewed by the examiner and is found to comply with the provisions of 37 CFR 1.63.

Drawings

3. The drawing(s) have been reviewed by the examiner and are found comply with the provisions of 37 CFR 1.81 to 1.85.

Specification

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Objections

5. Claim 10 is objected to because of the following informalities:

a. Claim 10 recites “the second isolator to ***receiver*** a sampled data bit" in line 16 of the claim (emphasis added). It appears Applicant intended to recite “the second isolator to ***receive*** a sampled data bit" (emphasis added). Appropriate correction is required.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 1 – 9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

8. Claim 1 recites the limitation "the first programmable component" in lines 5 – 6 of the claim. There is insufficient antecedent basis for this limitation in the claim.

The Examiner has interpreted the limitation as referring to the “first component coupled to the bus” recited earlier in the claim.

9. Claims 2 – 9 are also rejected for inheriting the deficiencies of parent claim 1.

10. Claim 15 recites the limitation "the data frames" in lines 2 – 3 of the claim. There is insufficient antecedent basis for this limitation in the claim.

Applicant is requested to verify the dependency of claim 15 from only claim 10. It appears that Applicant may have intended claim 15 to depend from claims 13 or 14, as claims 13 and 14 have proper antecedent basis for every limitation of claim 15.

11. Claim 15 recites the limitation "the serial port number" in line 5 of the claim. There is insufficient antecedent basis for this limitation in the claim.

Applicant is requested to verify the dependency of claim 15 from only claim 10. It appears that Applicant may have intended claim 15 to depend from claims 13 or 14, as claims 13 and 14 have proper antecedent basis for every limitation of claim 15.

12. Claim 15 has not been further considered on the merits because of its numerous deficiencies and suspected dependency error.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

13. Claims 1 – 2, 5, and 10 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent No. 6,965,366 (hereinafter Osborne).

As per claim 1, Osborne teaches a serial line circuit comprising a bus (Figure 2 [Connection between Items 18 and 20]); a plurality of isolators interposed between two portions of the bus (Figure 2 Item 16, Col 4 Lines 17 – 20); a first component coupled to the bus, the first programmable component to transfer information via a first isolator of the plurality of isolators (Figure 2 Item 18); and a second component coupled to the bus,

the second component to transfer sampled information over the bus via a second isolator of the plurality of isolators (Figure 2 Item 20).

As per claim 2, Osborne also teaches wherein the plurality of isolators is a pair of isolators including the first isolator and the second isolator (Col 4 Lines 1 – 20).

As per claim 5, Osborne also teaches wherein the first component to receive serial data bits (Figure 3 Item 36), multiplex the received serial data bits by forming data frames each including a plurality of overhead bits along with a serial bit of the received serial data bits (Figure 3 Item 30, Col 4 Lines 56 – 67), and to transfer the overhead bits along with the serial bit to the second component over the bus via the first isolator (Figure 3 Item 63).

As per claim 10, Osborne teaches an electronic device comprising a plurality of serial port connectors (Figure 1 Item 14); and a serial line circuit coupled to the plurality of serial port connectors (Figure 1 Item 10), the serial line circuit comprises a first programmable component (Figure 2 Item 18), a second programmable component in communication with the plurality of serial port connectors (Figure 2 Item 20), a bus coupled to the first programmable component and the second programmable component (Figure 2 [Connection between Items 18 and 20]), a first isolator situated along the bus (Figure 2 Item 16), the first isolator to receive a serial data bit preceded by control information from the first programmable component for transfer to the second

programmable component (Col 4 Lines 56 – 67), and a second isolator situated along the bus (Figure 2 Item 16), the second isolator to receive a sampled data bit preceded by control information from the second programmable component for transfer to the first programmable component (Figure 5 Item SD_{LS} and Item 62).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,965,366 (hereinafter Osborne) in view of Applicant's Admitted Prior Art (hereinafter AAPA).

As per claim 6, Osborne teaches the system as described per claim 5 (see rejection of claim 5 above.

Osborne does not teach wherein the first component receives the serial data bits from a plurality of serial Universal Asynchronous Receiver Transmitters (UARTs).

However, AAPA teaches a system in which UARTs supply serial data which is then transmitted through isolators (AAPA; Figure 1; Paragraphs [0002] – [0004])

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Osborne to include the

UARTs because doing so allows for conversion of data into a serial bitstream (AAPA; Paragraph [0004]).

15. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (hereinafter AAPA) in view of US Patent Application Publication No. 2004/0228629 (hereinafter Harris).

As per claim 16, AAPA teaches receiving a plurality of serial data bits (AAPA; Figure 1, Paragraph [0004]); and transferring the serial data bits over an interconnect through isolators to serial port connectors (AAPA; Figure 1, Paragraphs [0004] – [0006]).

AAPA does not teach multiplexing the plurality of serial data bits in order to transfer the serial data bits over an interconnect through a single isolator; recovering each of the plurality of serial data bits; and determining a serial port connector for each of the serial data bits.

However, Harris teaches using a multiplexer to send data from multiple lines through a single device on a single line instead of an array of devices on multiple lines, and using a demultiplexer to reroute the data from the single line back to multiple lines (Harris; Figure 8, Paragraph [0058]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of AAPA to include the multiplexing because doing so allows for reduction in component costs (Harris; Paragraph [0058]).

16. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (hereinafter AAPA) in view of US Patent Application Publication No. 2004/0228629 (hereinafter Harris) and further in view of US Patent No. 6,965,336 (hereinafter Osborne).

As per claim 17, AAPA in combination with Harris teaches the method as described per claim 16.

AAPA in combination with Harris does not teach wherein the multiplexing of the plurality of serial data bits comprises generating control information for each serial data bit of the plurality of data bits and transferring the control information along with a corresponding serial data bit immediately after each other.

However, Osborne teaches multiplexing data with control information and transmitting the control information along with the data (Osborne; Col 4 Lines 56 – 67).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of AAPA in combination with Harris to include the control information because doing so allows for data transmission without need for a recovery scheme at a receiver (Osborne; Col 4 Lines 43 – 51).

Allowable Subject Matter

17. Claims 3 – 4, and 7 – 9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the

limitations of the base claim and any intervening claims and to overcome the rejection(s) under 35 U.S.C. 112 2nd Paragraph set forth in this Office action.

Claim 3 would be allowable because the prior art of record fails to teach or suggest alone or in combination ***wherein the first component is a programmable component being a field programmable gate array (FPGA) to multiplex serial data received from a plurality of serial Universal Asynchronous Receiver Transmitters (UARTs) and to transfer the serial data over the bus via the first isolator***, as required by dependent claim 3, ***in combination with the other recited claim limitations*** (emphasis added). The prior art of record teaches multiplexing serial data with overhead data (Osborne; Col 4 Lines 56 – 67) by communications interface circuitry and transferring serial data by the first isolator, but does not teach wherein the first component is an FPGA and the serial data is received from a plurality of UARTs.

Claim 4 is also objected to as depending from claim 3 which is objected to as allowable above.

Claim 7 would be allowable because the prior art of record fails to teach or suggest alone or in combination ***wherein the overhead bits include a serial port number to identify a serial line connector to receive the serial bit corresponding to the overhead bits***, as required by dependent claim 7, ***in combination with the other recited claim limitations*** (emphasis added). The prior art of record teaches including overhead bits in with a serial data transmission (Osborne; Col 4 Lines 56 –

67), but does not teach wherein the overhead bits include a serial port number identifying a serial line connector to receive the serial bit.

Claims 8 and 9 are also objected to as depending from claim 7 which is objected to as allowable above.

18. Claims 11 – 12, and 18 – 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 11 would be allowable because the prior art of record fails to teach or suggest alone or in combination ***wherein the first component is a programmable component being a field programmable gate array (FPGA) to multiplex serial data received from a plurality of serial Universal Asynchronous Receiver Transmitters (UARTs) and to transfer the serial data over the bus via the first isolator***, as required by dependent claim 11, ***in combination with the other recited claim limitations*** (emphasis added). The prior art of record teaches multiplexing serial data with overhead data (Osborne; Col 4 Lines 56 – 67) by communications interface circuitry and transferring serial data by the first isolator, but does not teach wherein the first component is an FPGA and the serial data is received from a plurality of UARTs.

Claim 12 is also objected to as depending from claim 11 which is objected to as allowable above.

Claim 13 would be allowable because the prior art of record fails to teach or suggest alone or in combination ***wherein the first programmable component of the serial line circuit to receive serial data bits including the serial data bit, to multiplex the received serial data bits by forming data frames, one of the data frames including a serial port number along with the serial data bit, and to transfer the serial port number along with the serial data bit to the second programmable component over the bus via the first isolator***, as required by dependent claim 13, ***in combination with the other recited claim limitations*** (emphasis added). The prior art of record teaches multiplexing data bits with control information (Osborne; Col 4 Lines 56 – 67), but does not teach including a serial port number along with the serial bit and transferring the serial port number along with the serial bit to the second component over the bus via the first isolator.

Claim 14 is also objected to as depending from claim 13 which is objected to as allowable above.

Claim 18 would be allowable because the prior art of record fails to teach or suggest alone or in combination ***wherein a transmission rate of the interconnect exceeds a transmission rate of at least one interconnect providing the corresponding serial data bit by a factor of at least one-hundred***, as required by dependent claim 18, ***in combination with the other recited claim limitations*** (emphasis added). The prior art of record teaches reducing multiple incoming transmission lines to a single transmission line, but does not teach that the transmission

rate of the single transmission line is at least one hundred times faster than any one of the multiple incoming transmission lines.

Claims 19 and 20 are also objected to as depending from claim 18 which is objected to as allowable above.

Conclusion

19. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. US Patent No. 5,896,415 - Teaches that a bi-directional isolator consists of two isolators, one for each direction in Figure 4.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to RICHARD FRANKLIN whose telephone number is (571)272-0669. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571) 272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Richard Franklin
/RBF/
Patent Examiner
Art Unit 2181

/Alford W. Kindred/
Supervisory Patent Examiner, Art Unit 2181